Online Algorithm for FoCal

Tatsuya Chujo

Univ. of Tsukuba

Mini-workshop on next generation DAQ

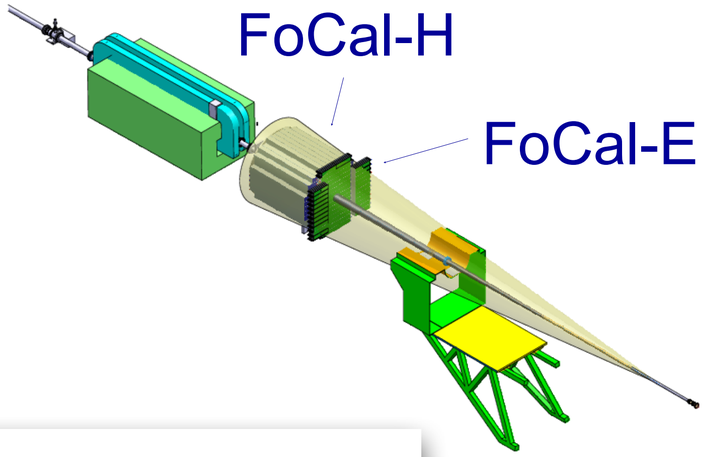
March 16, 2020, Campus Innovation Center Tokyo,

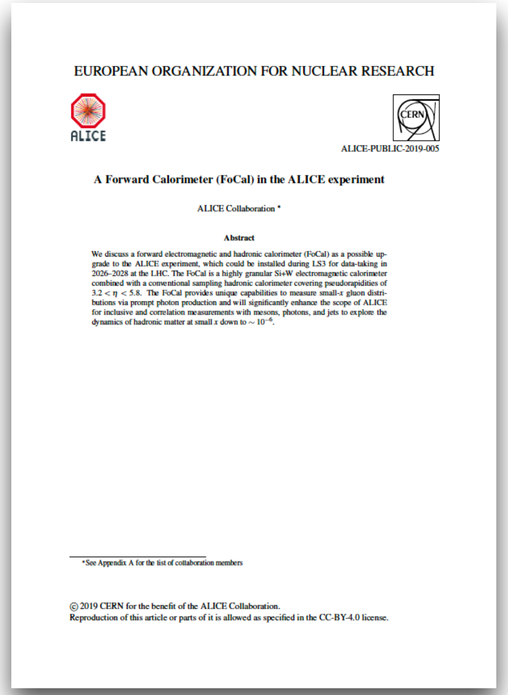
Tamachi Tokyo, Japan

筑波大学
University of Tsukuba

ALICE FoCal status

- ALICE public note (~FoCal LoI) has been submitted to CDS, ALICE-PUBLIC-2019-005, on Nov. 1st, 2019
  - https://cds.cern.ch/record/2696471
- Discussed the ALICE FoCal at LHCC meeting on Nov. 2019 and Feb. 2020.
- **ALICE internal review of FoCal: Jan. 14th, 2020**.
  - plan: then submission of the FoCal LoI to LHCC, and will **discuss at the LHCC June 2020 meeting for the approval**.





EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

ALICE

CERN

ALICE-PUBLIC-2019-005

A Forward Calorimeter (FoCal) in the ALICE experiment

ALICE Collaboration *

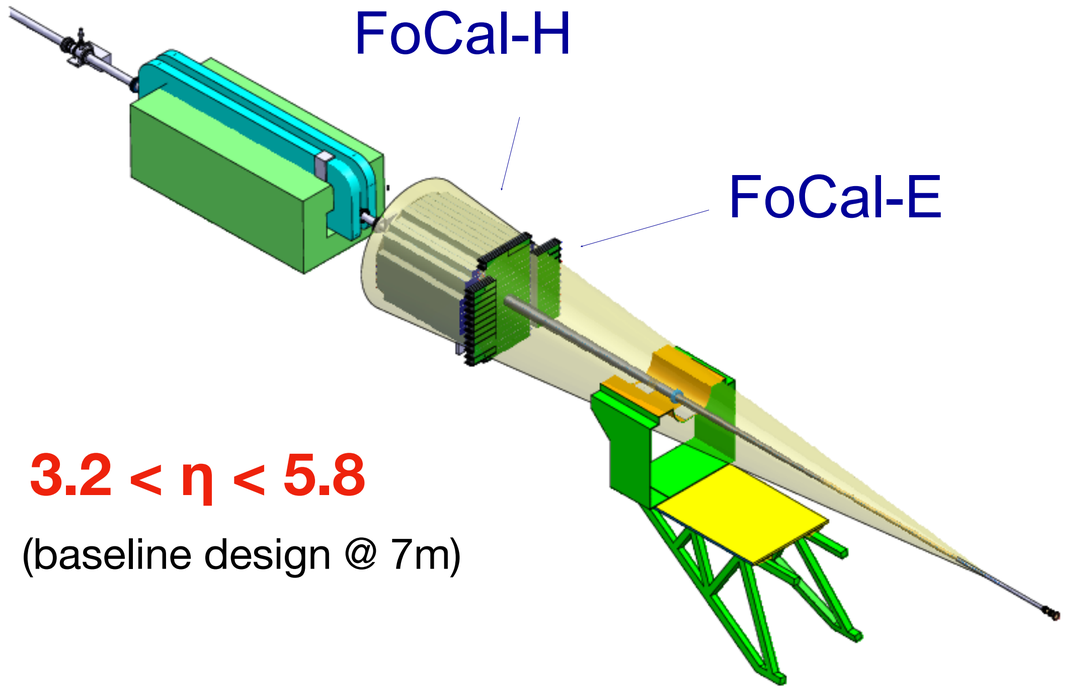
Abstract

We discuss a forward electromagnetic and hadronic calorimeter (FoCal) as a possible upgrade to the ALICE experiment, which could be installed during LS3 for data-taking in 2026–2028 at the LHC. The FoCal is a highly granular Si-W electromagnetic calorimeter combined with a conventional sampling hadronic calorimeter covering pseudorapidities of $3.2 < \eta < 5.8$. The FoCal provides unique capabilities to measure small-x gluon distributions via prompt photon production and will significantly enhance the scope of ALICE for inclusive and correlation measurements with mesons, photons, and jets to explore the dynamics of hadronic matter at small x down to $\sim 10^{-6}$.

*See Appendix A for the list of collaboration members

The FoCal proposal

FoCal-E: high-granularity Si-W sampling calorimeter for photons and π^0
FoCal-H: conventional Cu-Sc sampling calorimeter for photon isolation and jets



$3.2 < \eta < 5.8$

(baseline design @ 7m)

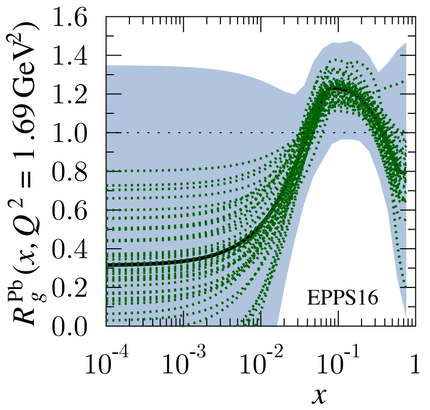
Observables:

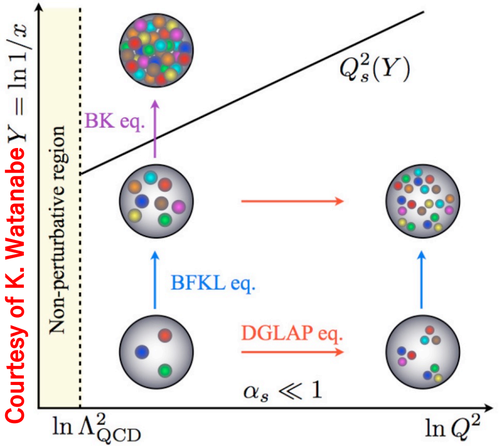
- π^0 (and other neutral mesons)
- Isolated photons
- Jets (and di-jets)
- J/ψ (Y) in UPC
- W, Z maybe possible
- Event plane and centrality

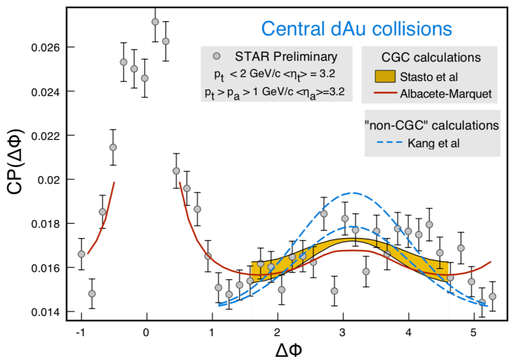
Advantage in ALICE:
forward region nearly not instrumented;
'unobstructed' view of interaction point

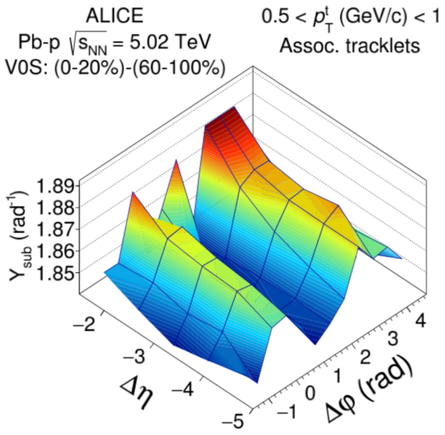
Physics goals

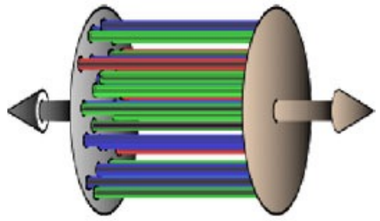
- **Quantify nuclear modification of the gluon density at small-x**
  - Isolated photons in pp and pPb collisions
- **Explore non-linear QCD evolution**
  - Azimuthal π^0-π^0 and isolated photon-π^0 (or jet) correlations in pp and pPb collisions
- **Investigate the origin of long range flow-like correlations**
  - Azimuthal π^0-h correlations using FoCal and central ALICE (and muon arm?) in pp and pPb collisions
- **Explore jet quenching at forward rapidity**
  - Measure high p_T neutral pion production in PbPb

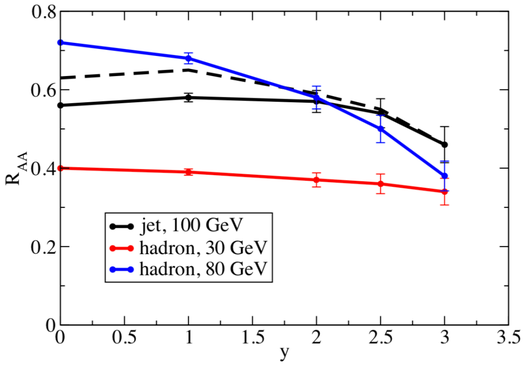










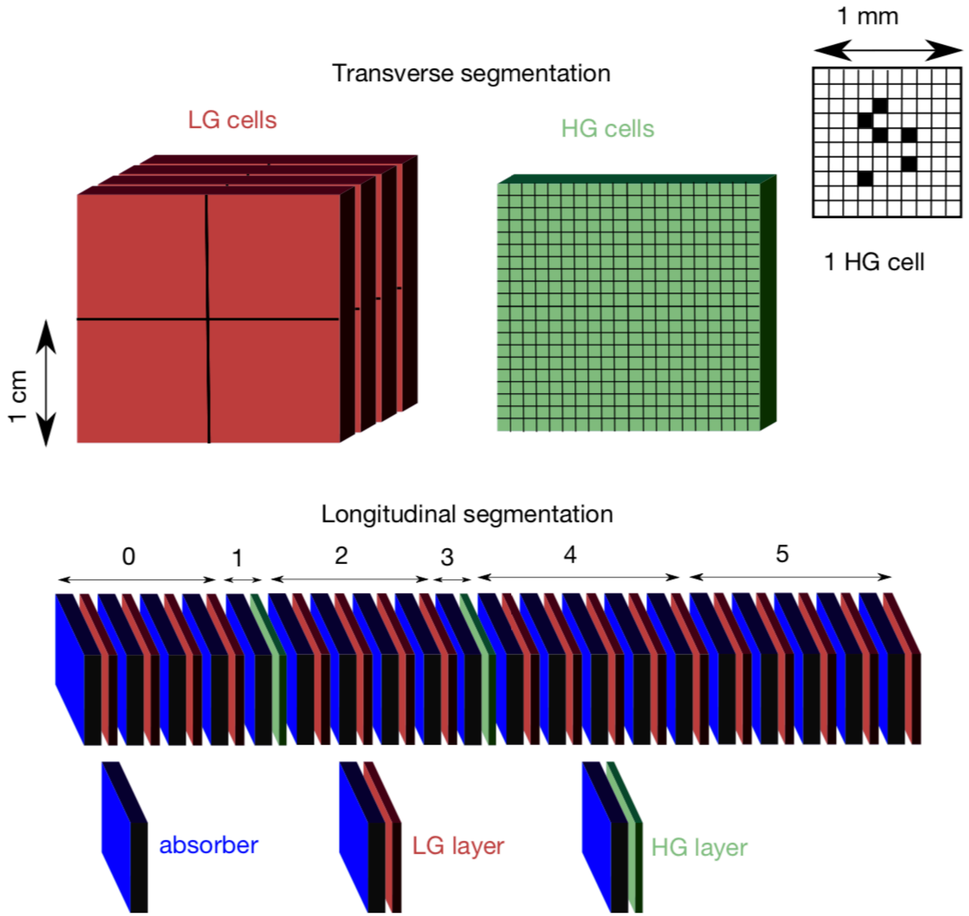


Key questions

* How QGP is created in heavy ion collisions and how thermalized?

* Is there any difference between QGP in the early universe and QGP produced in heavy ion collisions?

FoCal-E design



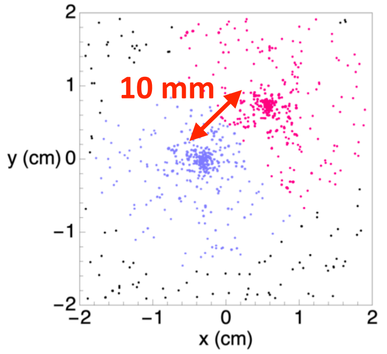
Studied in simulations 20 layers:
W(3.5 mm ≈ $1X_0$) + silicon sensors
Two types: Pads (LG) and Pixels (HG)

- Pad layers provide shower profile
- Pixel layers provide position resolution to resolve shower overlaps

Main optimization:

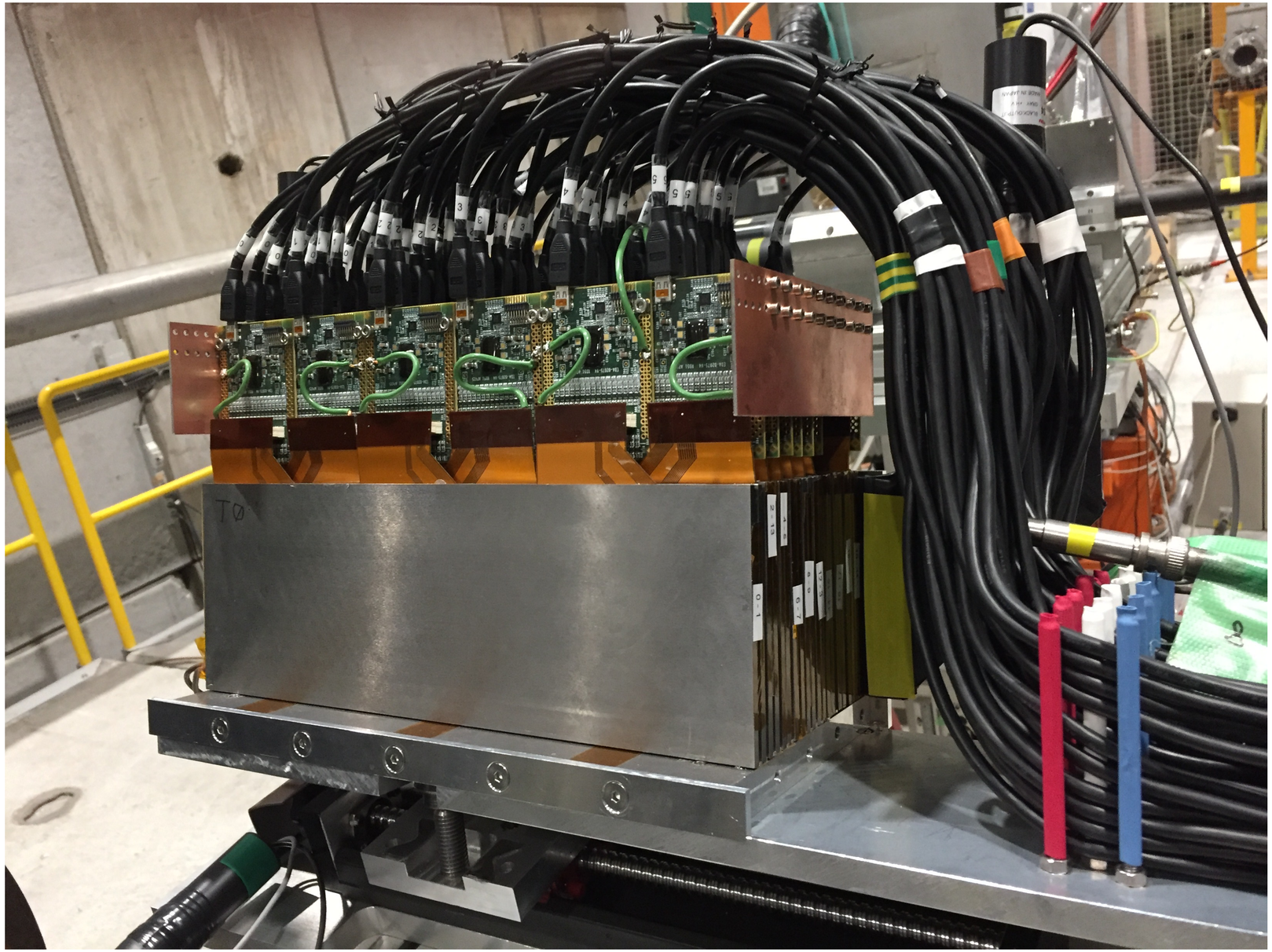
- Number of pixel layers and location
- Number of pad layers
- Maximum separation between layers

- Main challenge: Separate γ/π^0 at high energy
  - Two photon separation from π^0 decay (10 GeV, η=4.5) ~2mm
  - Needs small Molière radius and high granularity readout
  - Si-W calorimeter with effective granularity ≈ 1mm^2

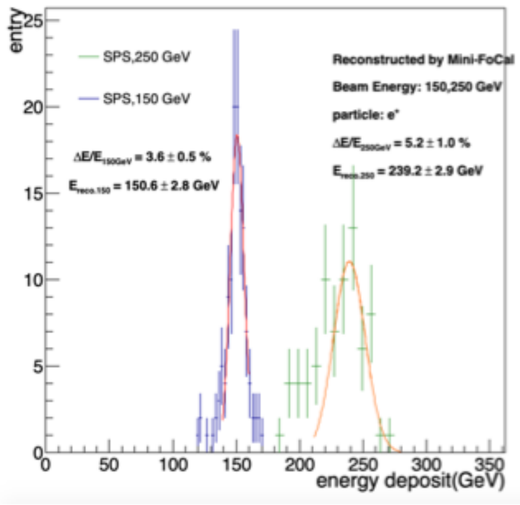


5.4 GeV electron, pileup event

mini-FoCal (FoCal-E, PAD only)



Y. Minato



ΔE/E = 3.6 %
@ 150 GeV/c , e^- (SPS)

- Built in Tsukuba, and shipped to CERN for test beam and ALICE test in 2018
- APV25 hybrid + SRS for readout

Slides from “ALICE FoCal review” on Jan. 14, 2020,
by Fatah Rarbi (LPSC Grenoble) “PAD Readout Design”

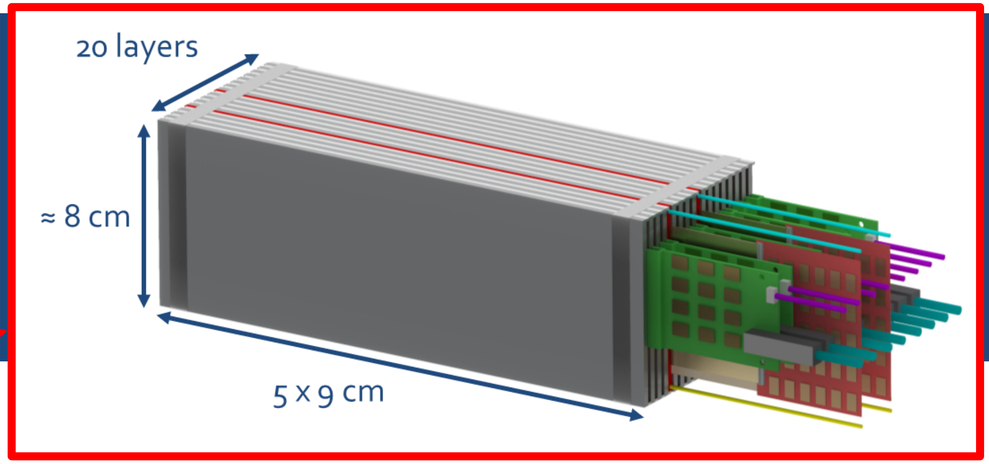
PAD READOUT DESIGN

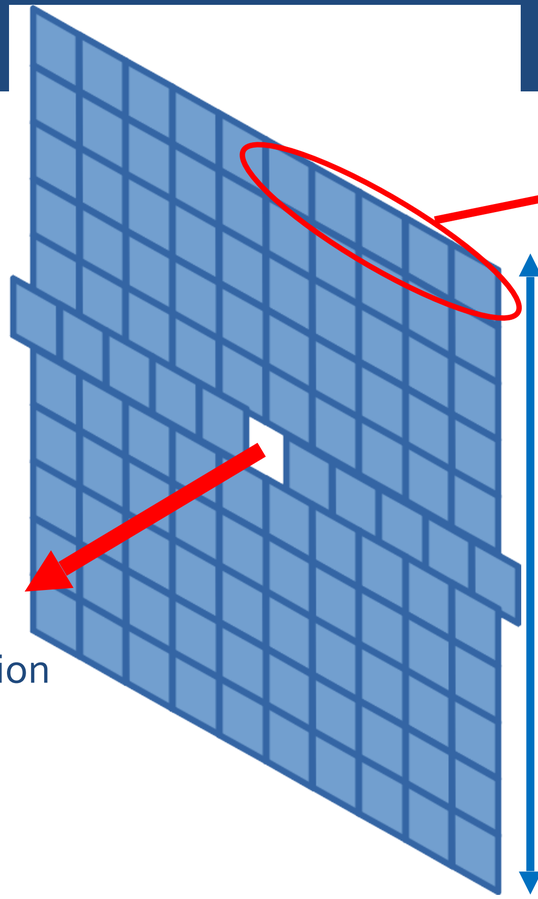
Fatah RARBI

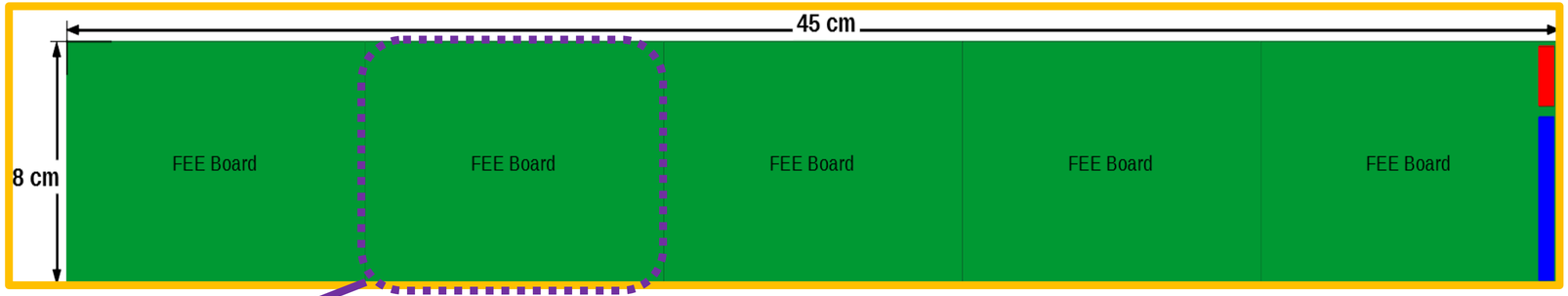
Olivier Bourrion, Rachid Guernane, Damien Tourres, Christophe Hoarau

GRENOBLE | MODANE

FEW DEFINITIONS







Module:

Composed of 18 **pad-layers** + 2 MAPS layer

Pad layers:

Composed of 5 **pads sensors** + associated FEE-PCB

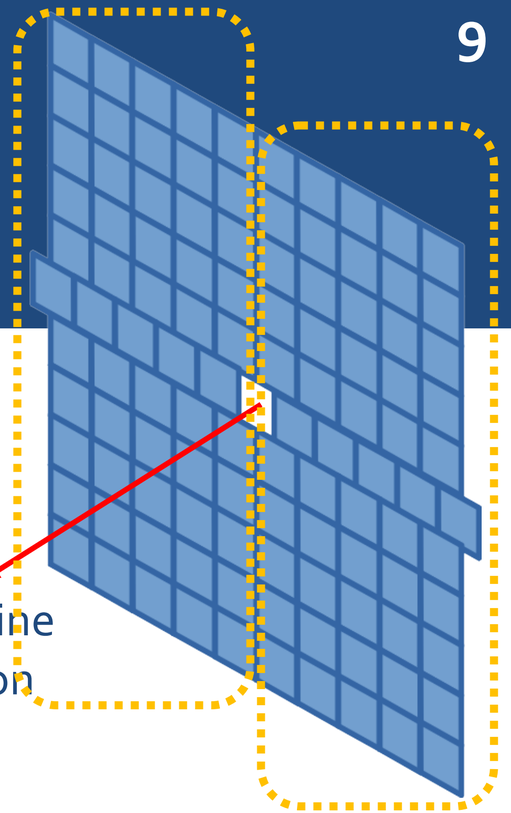
1 FEE-PCB linked to readout PCB (Aggregator board)

Si-pad:

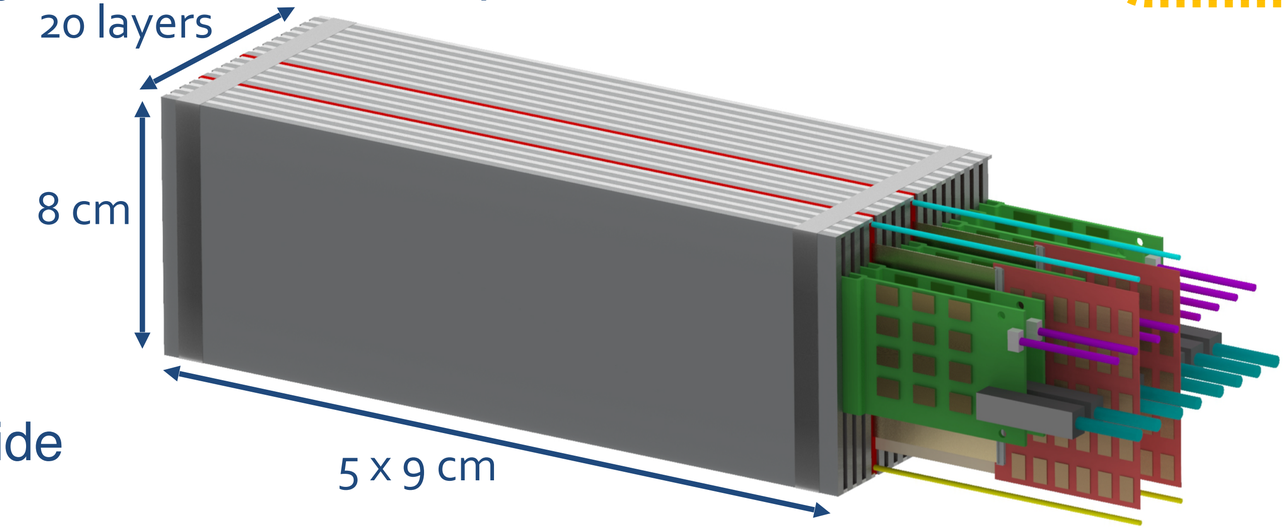
Built up from silicon pad sensors with a granularity of 1 x 1 cm^2

Sensitive area of 9 x 8 cm^2 for each sensor: total of **72 pixels**

FOCAL-E DESIGN CONCEPT

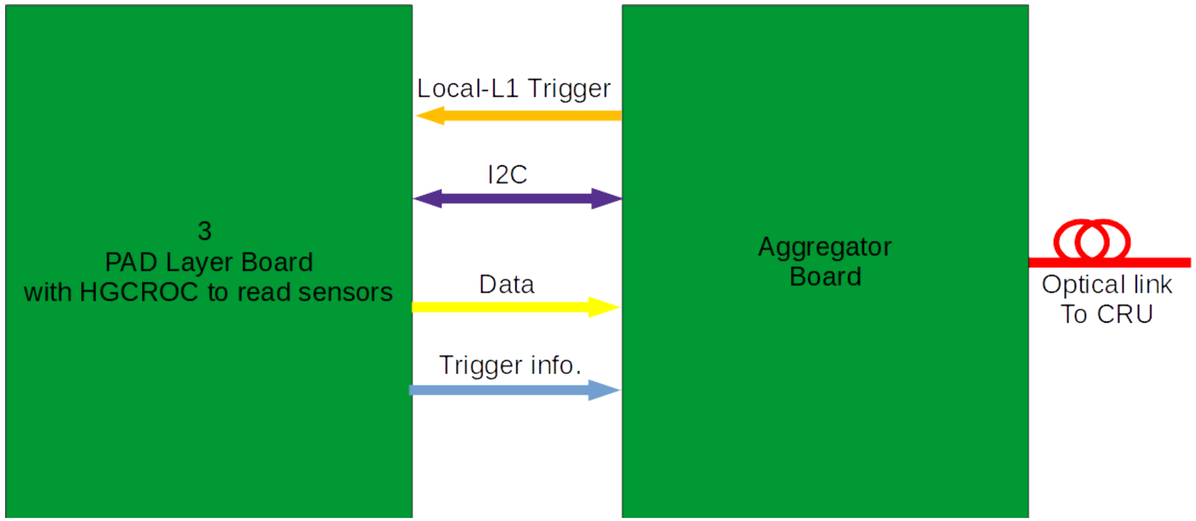


- Focal-E detector is designed with 22 modules: **2 x 11 modules**
- A single FoCal-E module, containing 20 layers of W converter and Si sensors
  - **18 of the layers consist of 5 pad sensors of 9 x 8 cm²**
  - 2 layers use pixel sensors (MAPS layer of 9 x 6 ALPIDE pixel sensor chips)
  - The total sensitive area of the module will be approx. 45 x 8 cm²
  - All connections for readout, bias voltage, power and cooling are routed outside
  - 2 modules can be stacked side-by-side



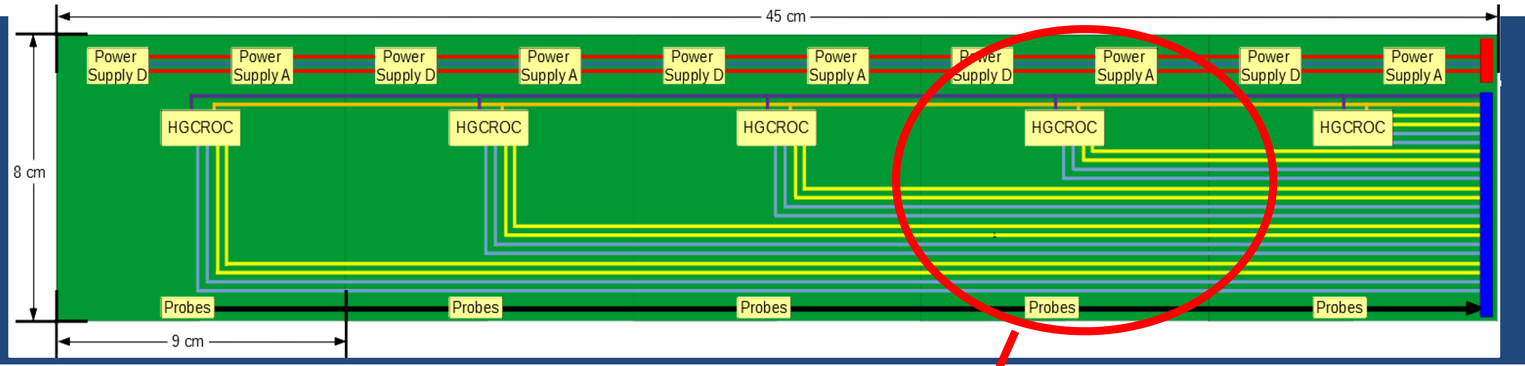
FULL ELECTRONIC ARCHITECTURE

- Pad Layer board is based in HGCROC: designed by OMEGA-IN2P3 for HGCAL in CMS
  - Will be used as is
- Aggregator Board gathers data and trigger information from pad layer board
  - Based in FPGA
  - Can generate Local-L1 trigger from Trigger info provided by HGCROC

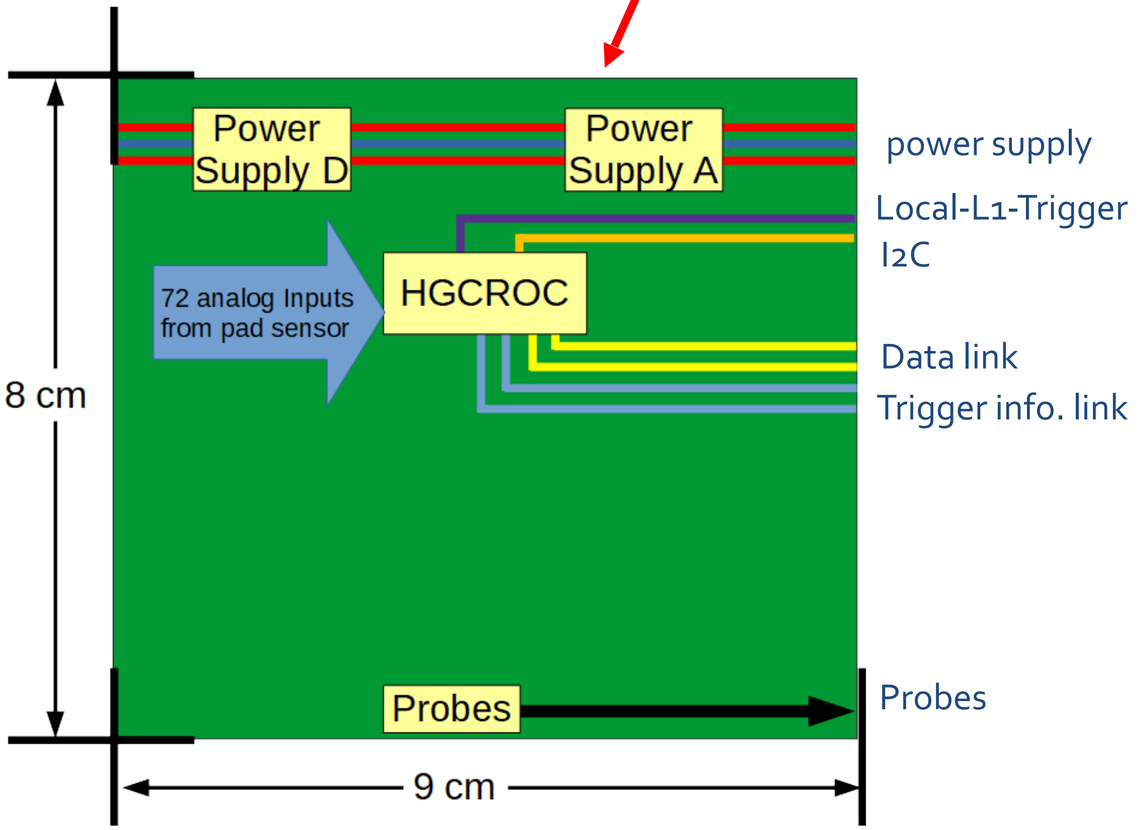


Slides by F. Rarbi at FoCal review (2020)

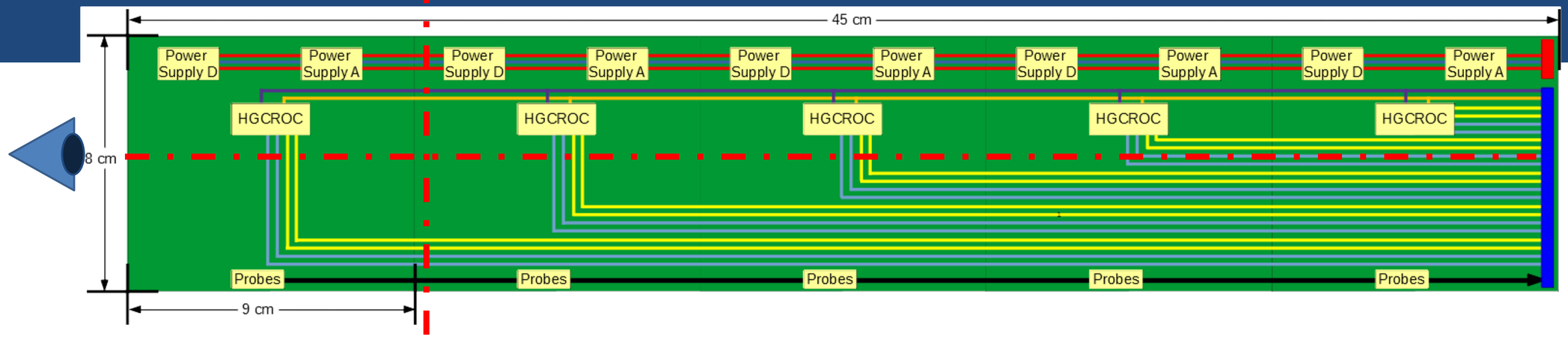
PAD-LAYER: PROPOSED FEE ARCHITECTURE

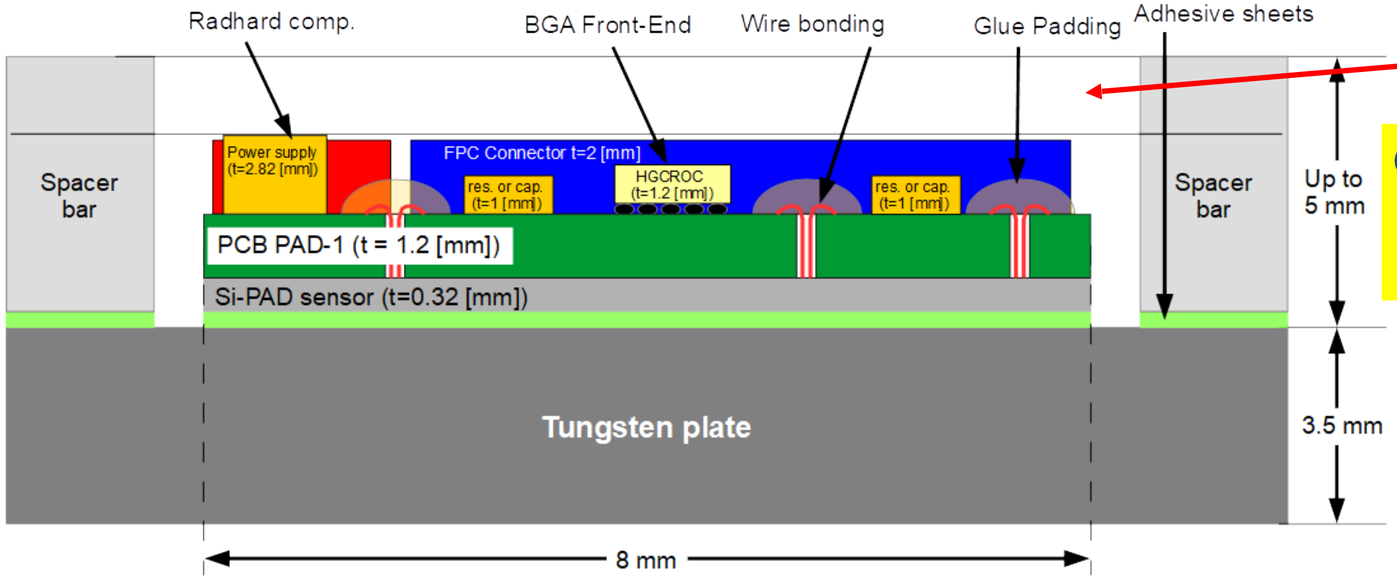


- FEE architecture :
  - PCB of 8 x 45 cm² with 5 embedded "HGCROC"
  - Analog signals from each pad sensors (72 pixels) will be read out by the HGCROC front-end chip which includes a charge sensitive amplifier-shaper and digitized to ship the data on a standard digital connection
  - Probes:
    - Temperature
    - Analog Power consumption
    - Digital Power consumption
  - Local power converter for cleaning power supplies



PAD-LAYER DESIGN





few mm of margin for cooling

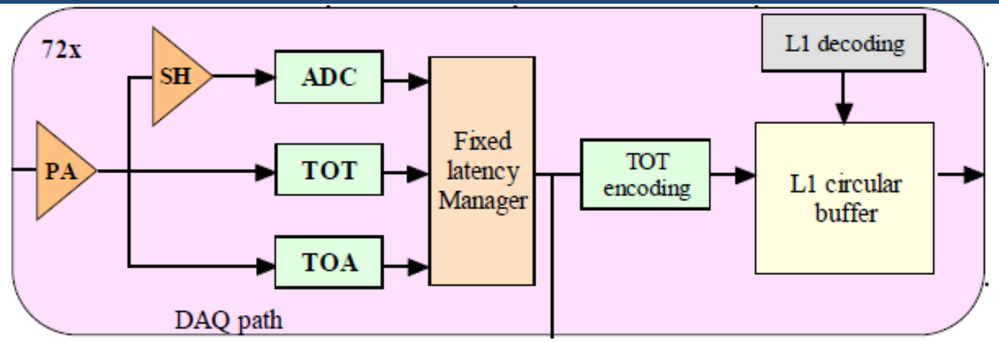
CALICE info.:

Tungsten plate not enough for heat dissipation

Passive cooling with copper sheet (see backup)

HGCROC: SPECIFICATION

- FoCal
  - Dynamic range:
    - 3fC/MIP ➔ 1MIP up to 2500MIP
    - 3fC up to 7.5pC
- HGCROC:
  - Charge measurement through 10b, 40MSPs ADC (up to 100fC) + TOT (0.1-10pC)
  - Both TOT and TOA measurements are handle by a dedicated TDC block
    - **TOT** ("Time Over Threshold") for charge measurement (+ ADC for low level signal)
    - **TOA** ("Time Of Arrival") for timing measurement

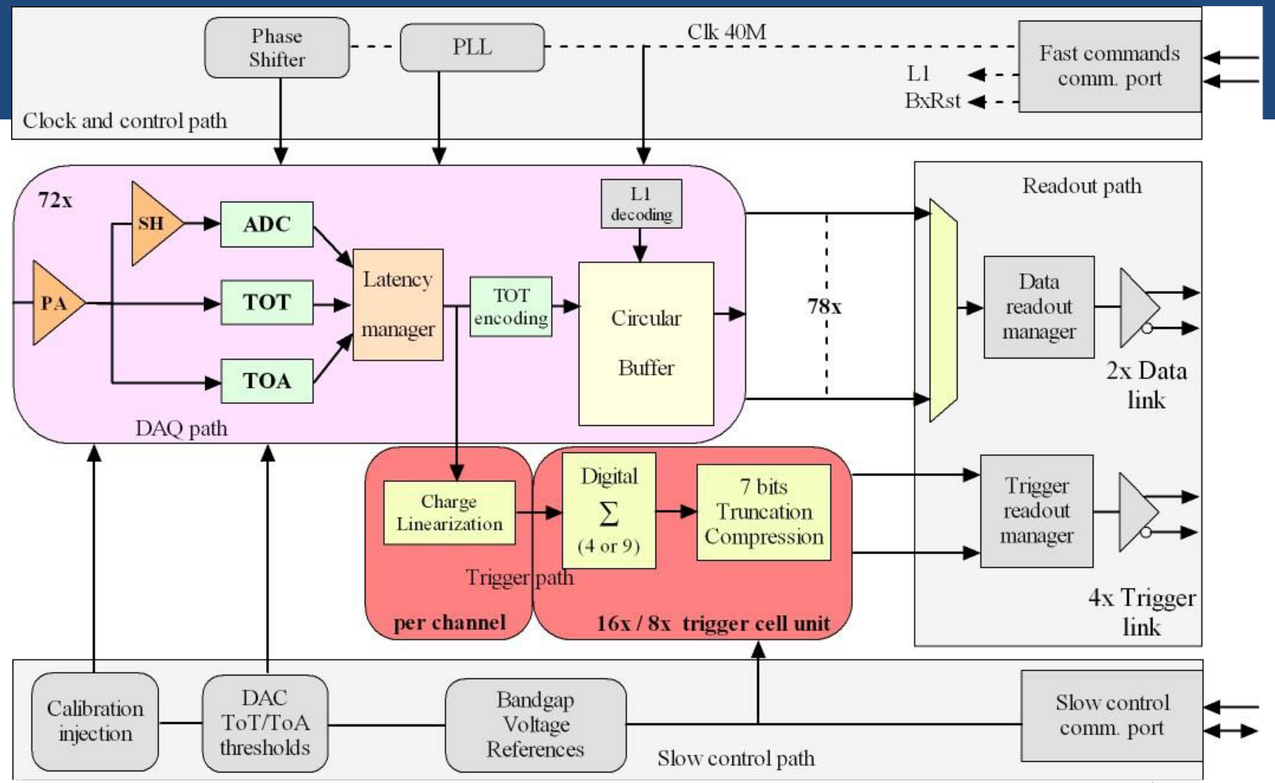


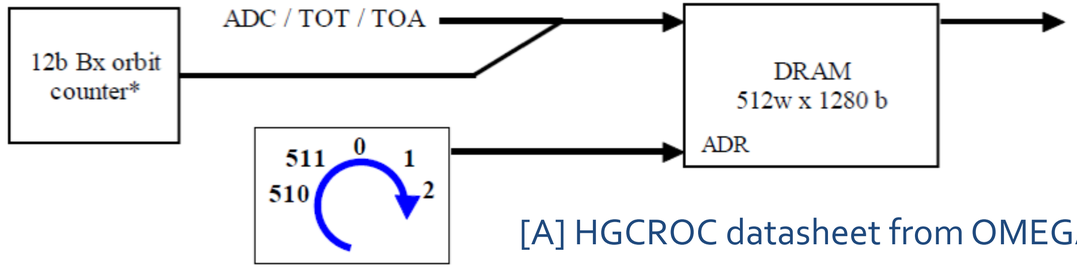
TDC ToA specifications	
Resolution	about 25 ps RMS
Range	10 bits over 25 ns
Conversion rate	> 40 MHz (bunch clock)
Power consumption	< 2 mW / channel
Area	Pitch 120 µm
Technology	TSMC 130 nm
Temperature	-30 °C

TDC ToT specifications	
Resolution	< 50 ps RMS
Range	12 bits over 2-200 ns
Min time between hits	25 ns
Power consumption	< 2 mW / channel
Fixed latency	12 clock periods
Technology	TSMC 130 nm
Area	Pitch 120 µm
Temperature	-30 °C

HGCROC: DESCRIPTION

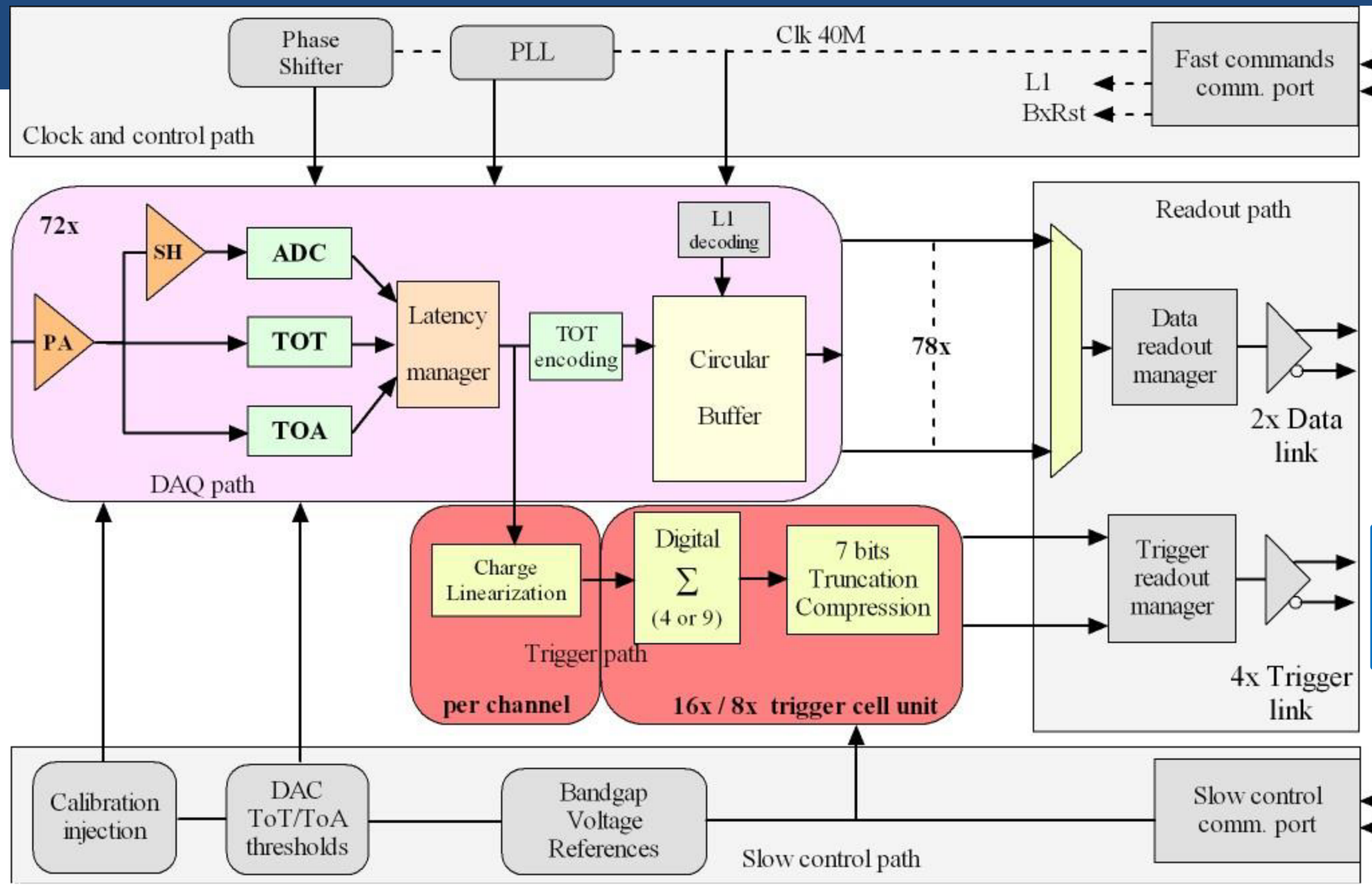
- 72 channels + 4 channels for common mode subtraction + 2 special calibration channels
- 32b Digital Data continuously stored in 512 length DRAM @40MHz
  - 72 ch. x 32b x 40MHz: **huge data volume**
  - ➔ Only **Local-L1-triggered** data are read out
- Idle packet is continuously sent out when no L1-trigger is activated
- The data processing for the trigger "information" path
  - 32b: 4b header + 7b x 4
  - Sum of 4 or **9 channels** depending on the sensor



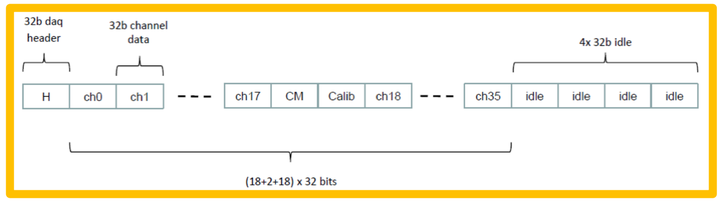


[A] HGCROC datasheet from OMEGA group

HGCROC: DATA READOUT & TRIGGER

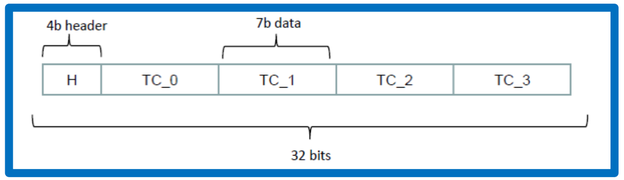


Feedback of Local-L1 trigger to readout data stored in DRAM



1376b → to be readout at 1.28Gb/s

→ 1.075 µs (≈930kHz)



charge sum (TC_X) produced @40MHz and sent @1.28Gb/s

Time between 2 successive local-L1-Trigger: 1.075µs ≈ 1µs

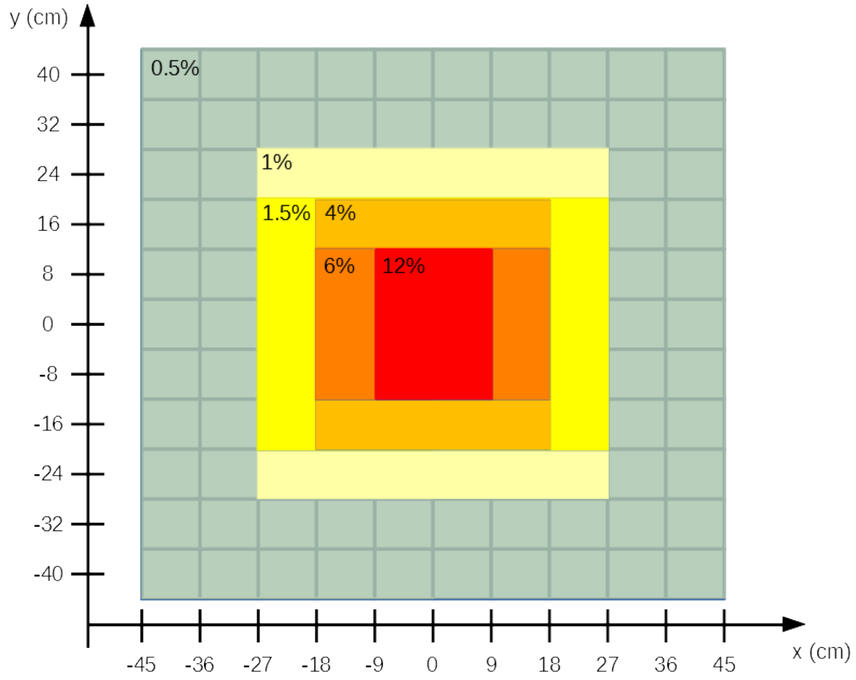
OCCUPANCY: ASSOCIATED DATA RATE

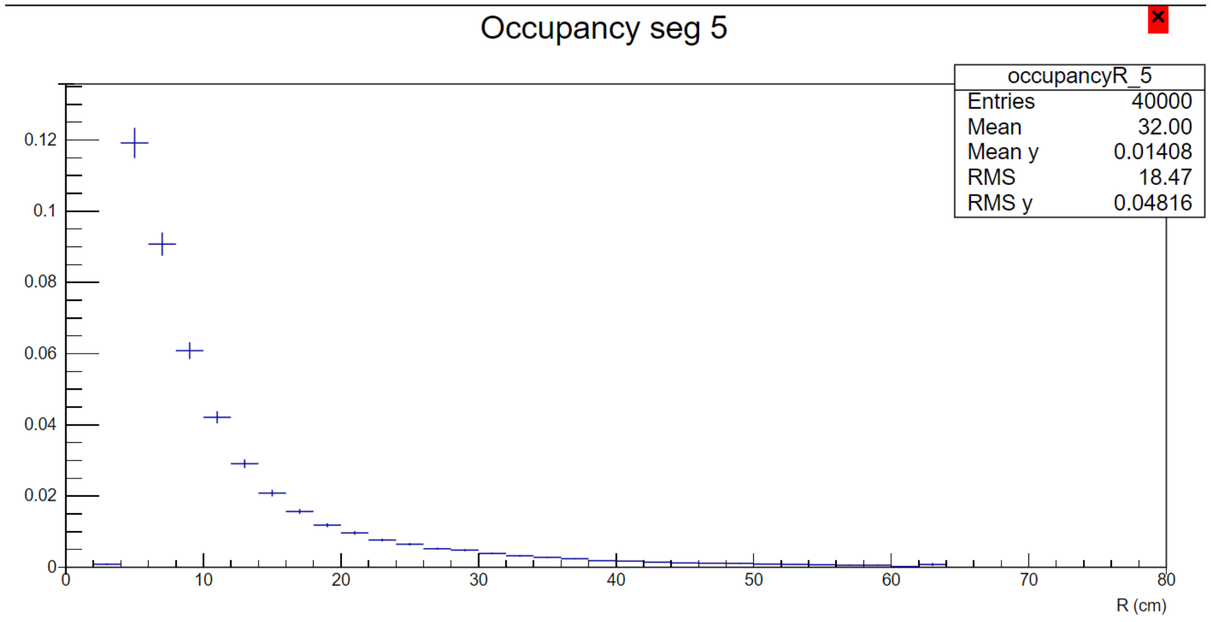
- 1 pad-layer is composed of 5 pads (Si-sensor and the "PCB" with embedded FEE)
- Estimation of the data rate for the several pad layers (x and y axis)
- Data format for each channel defined by HGCROC:
  - 32 bits (ADC (10b) + TOA (10b) + TOT (12b))
- New data format according to the occupancy factor ➔ take into account the channel number (7 bit), the pad sensor (TBD), … for example

DATA RATE ESTIMATION FOR 1 SI PAD: PP COLLISIONS @1MHZ

- Example for 1 Si-pad sensor:
  - 1MHz counting rate, 72 pixels, 32 bit of data, 7 bit for channel number, header, calib., and common mode from HGCROC, 12% of occupancy:
    - We obtain a data rate of:

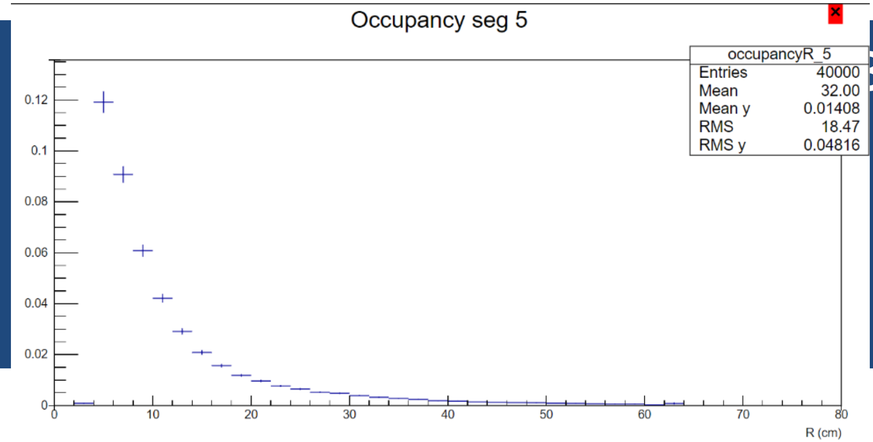
$$1MHz \times (32b + 0.12 \times 72 \times 32b + 0.12 \times 72 \times 7b) = \mathbf{368.96}Mb/s$$



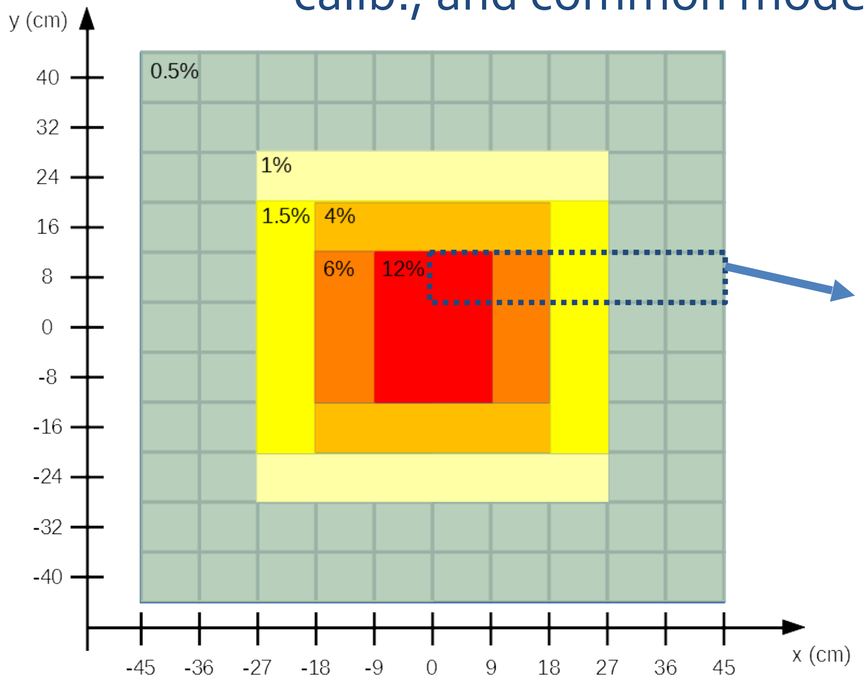


Slides by F. Rarbi at FoCal review (2020)

DATA RATE ESTIMATION: PP COLLISIONS @1MHZ



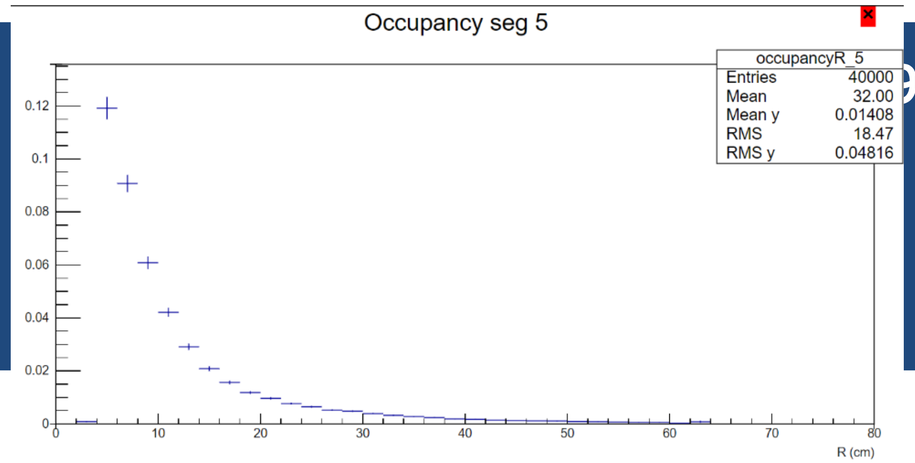
- Example for 1 pad layer:
  - 5 Si pad sensor, multiple occupancy factor
  - 1MHz counting rate, 72 pixels/pad-sensor, 32 bit of data, 7 bit for channel number, header, calib., and common mode from HGCROC, 12%, 6%, 1.5% and 0.5% of occupancy:



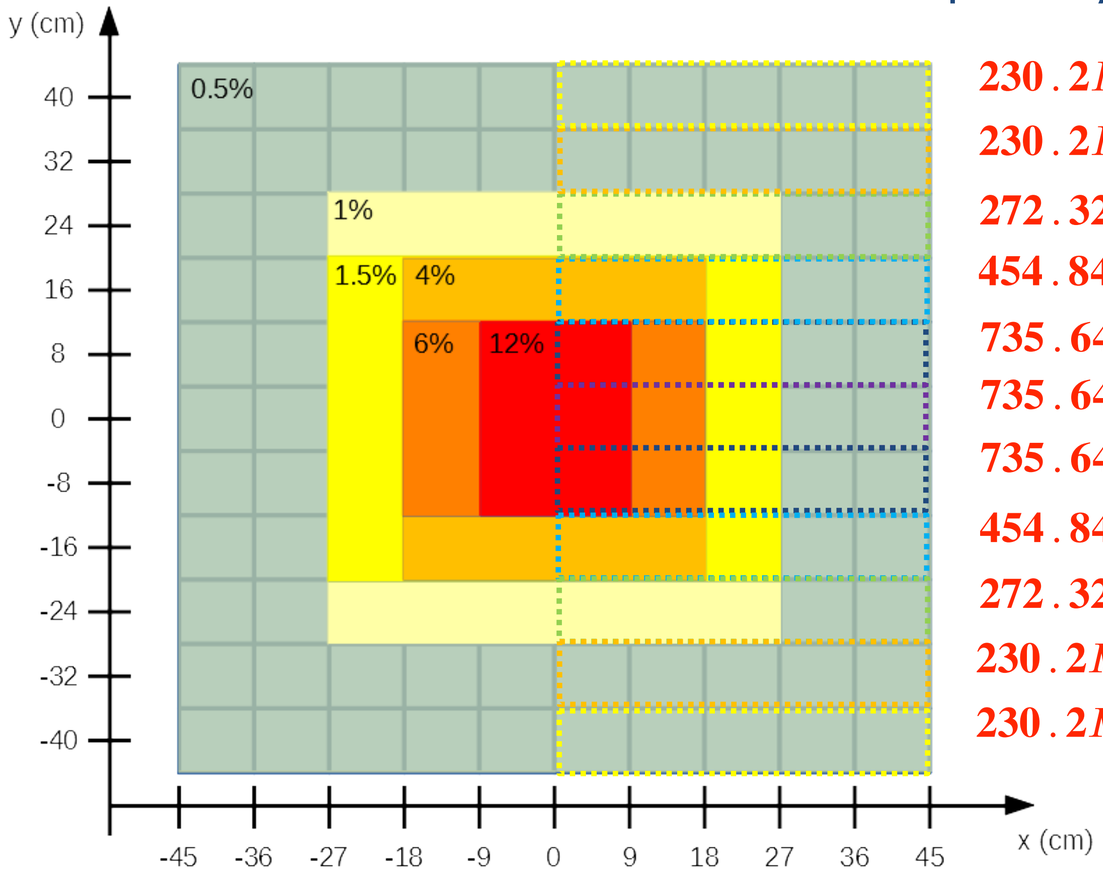
$$1MHz \times \left[\begin{array}{l} (32b + 0.12 \times 72 \times 32b + 0.12 \times 72 \times 7b) \\ + \left(32b + 0.06 \times 72 \times 32b + 0.06 \times 72 \times 7b\right) \\ + \left(32b + 0.015 \times 72 \times 32b + 0.015 \times 72 \times 7b\right) \\ + 2 \times \left(32b + 0.005 \times 72 \times 32b + 0.005 \times 72 \times 7b\right) \end{array} \right] = \mathbf{735.64}\,\boldsymbol{Mb/s}$$

Slides by F. Rarbi at FoCal review (2020)

DATA RATE ESTIMATION: PP COLLISIONS @1MHZ



- Data rate estimation for each pad layer



Possible to share GBT-FPGA to several pad layers

→ **Design for the maximum rate**

→ @3.2Gb/s with FEC (80b @40MHz)

→ @4.8Gb/s w/o FEC (112b @40MHz)

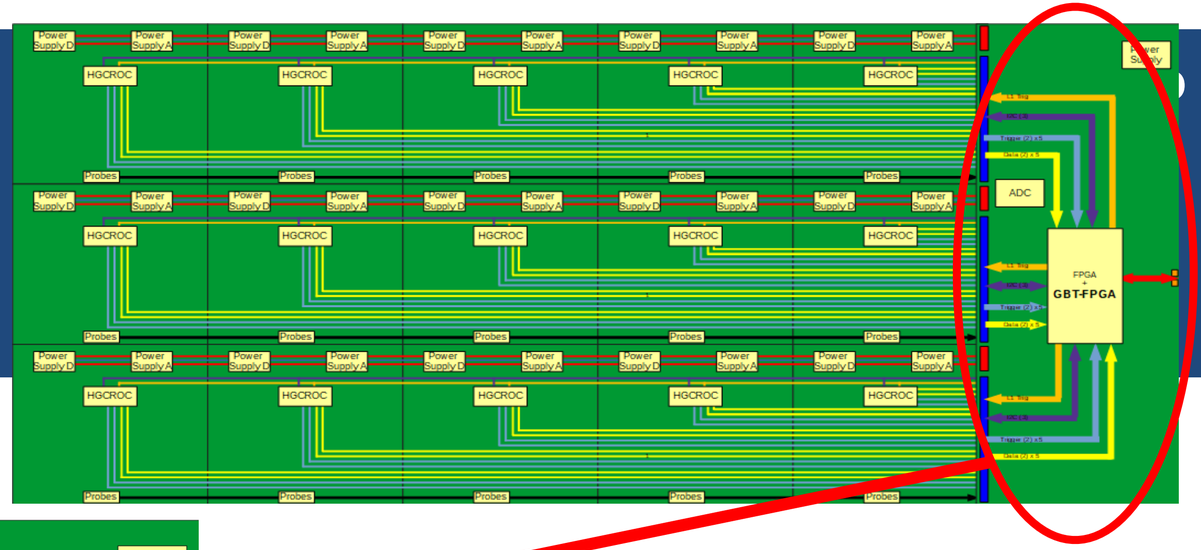
→ **Reduce the number of needed GBT-FPGA**

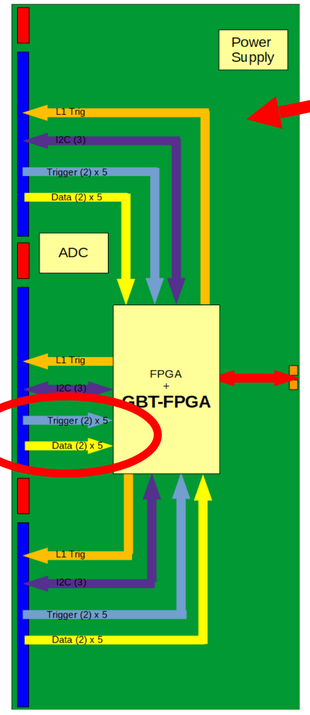
→ **Reduce the number of needed CRU**

Slides by F. Rarbi at FoCal review (2020)

FEE AGGREGATOR BOARD

- Example of 3 pad-layers connected to one aggregator board
- General power supply for the FEE-PCB pad layer
- ADC for monitoring purposes:
  - Probes measurement
    - Each pad layer needs 15 voltage measurements
- FPGA: input data @1.28Gb/s
  - GBT-FPGA: shared with other pad-layers
  - I2C slow control
  - Generate Local-L1-Trigger to be send to read out 1 Bx data or more
  - Modification of data format
  - Upgrade of the firmware
- Radiation tolerant design
  - FEE Aggregator board is about 45 cm away from the beam
  - Ultrascale technology expected to be more radhard
  - Should be OK (some private communication from ITS) but precise estimates still missing
- Heat dissipation of the aggregator board: **cooling is mandatory**





@1.28Gb/s

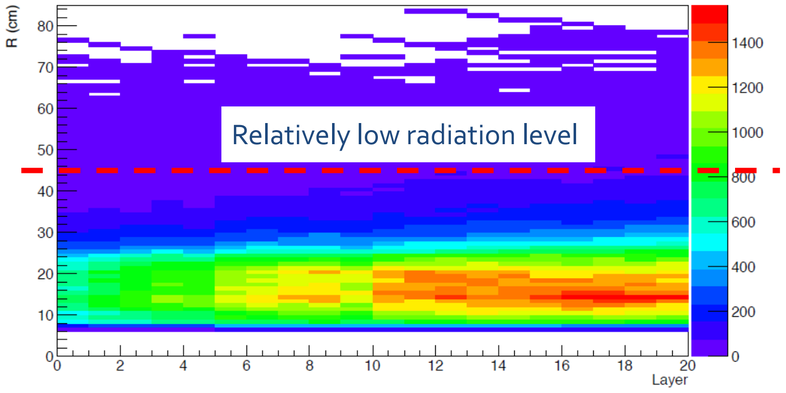
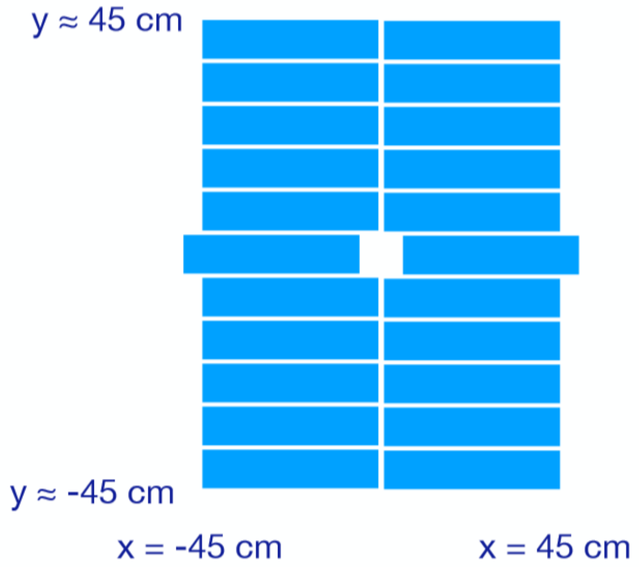


Fig. 52: Neutron flux (arbitrary units) in FoCal as a function of layer number and radial position. One layer corresponds to a thickness of approximately 1 X_0 in the z direction.

PAD LAYERS GATHERING

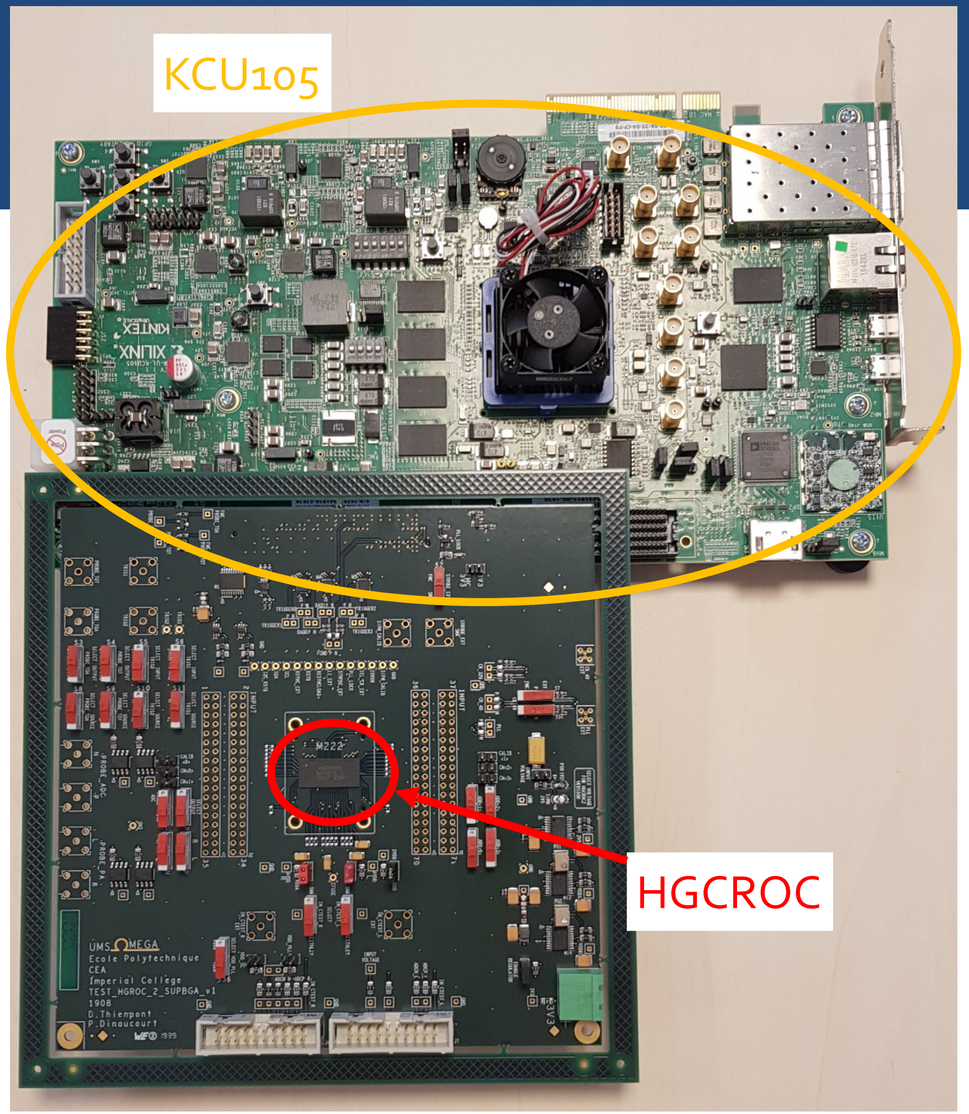
Occupancy	# modules	# pad-layers	Input Data rate per pad layer	# pad-layers/optical-link	
				@3.2Gb/s	@4.8Gb/s
12 % - 6% - 1.5% - 0.5%	6	108	735.64Mb/s	4	6
4% - 1.5% - 0.5%	4	72	454.84Mb/s	7	10
1% - 0.5%	4	72	272.32Mb/s	11	17
0.5%	8	144	230.2Mb/s	13	20
Total	22	396			



- Aggregator board connected to at most 3 pad-layers due to the limited number of FPGA I/O
  - Ex. : 3 pad-layers have a total of 120 signals @1.28Gb/s (data + trigger)
- According to possible arrangements for FoCal modules:
  - Choice to make on the number of pad-layers to be connected to the aggregator board
    - 3 different aggregator boards needed ➔ 180 FPGA
      - Aggregator board connected to 3 pad-layers
      - Aggregator board connected to 2 pad-layers
      - Aggregator board connected to 1 pad-layers

WORK IN PROGRESS

- HGCROC received from OMEGA group
- KCU105: Xilinx Dev. Kit already used in lab.
  - **Phase 1:** understand both Firmware and software
    - Work in progress to get used to operate the HGCROC chip
  - **Phase 2:** design a FEE board of pad-layers + an Aggregator board



FOCAL SCHEDULE @LPSC

FOCAL Planning @LPSC								
	2020				2021			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
HGCROC Understanding								
FEE PAD Layer: Prototype 0								
Test with Pad sensor								
FEE PAD Layer: Prototype 1								
Aggregator Board								
Test with Pad sensor								

HGCROC Understanding:

Define both firmware and software to get used to operate the HGCROC chip

FEE PAD Layer: Prototype 0:

Define the design of a development kit including ONE HGCROC and all other components as power supply, probes and holes to connect Si-pad sensor through wire bonding
This PCB can be connected to the KCU105

Test with pad sensor:

Analyzing FEE board: noise, crosstalk, …
Different Si-pad sensor could be tested

FEE PAD Layer: Prototype 1:

Define the design of the full FEE pad layer including the FIVE HGCROC

Aggregator Board:

Define the design of the aggregator board to be linked to the FEE PAD Layer (prototype 1) and includes FPGA and optical link

CONCLUSION (PAD READOUT)

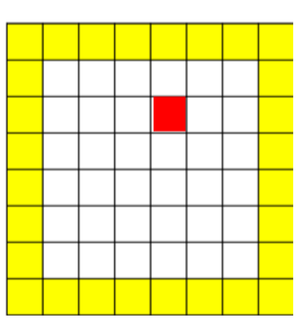
- FOCAL-E Detector
  - 22 modules
    - 1 modules composed of 20 layers: 18 pad layers + 2 MAPS (ALPIDE) layers
    - Pad layer: 5 pad sensors of 72, 1x1 cm^2 pixel + associated FEE
    - Each pad layers linked to an aggregator board with embedded FPGA for data gathering, I2C slow control and monitoring possibilities
  - By sharing readout parts (FPGA): only 180 FPGA could be used
    - The readout concept is a self-triggered mode with the FPGA providing the trigger decision
    - 8 CRU (24 optical fiber/CRU)
- Electronics to **design**, to **test** and to **validate**
  - 396 pad layers
  - 180 FEE aggregator board according to arrangement option for FoCal modules
    - 3 different aggregator boards

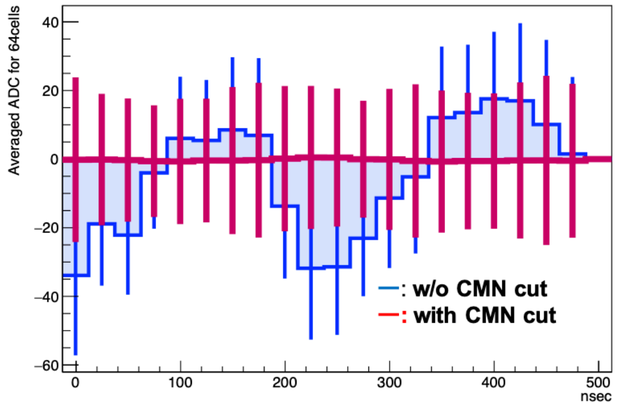
Possible online data processing for FoCal PAD

1. Pedestal subtraction and zero suppression
2. Removal of Common Mode Noise (CMN)
3. Signal selection (threshold) & clustering (2x2 or 3x3)
4. Longitudinal summing
5. (Trigger for high energy cluster)

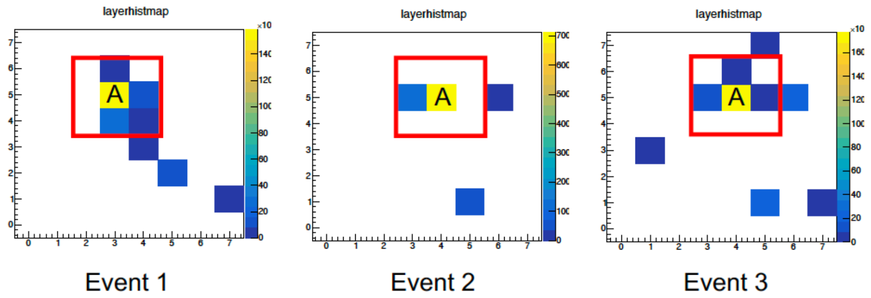
→ Aggregator board or CRU?

(a) Common mode noise

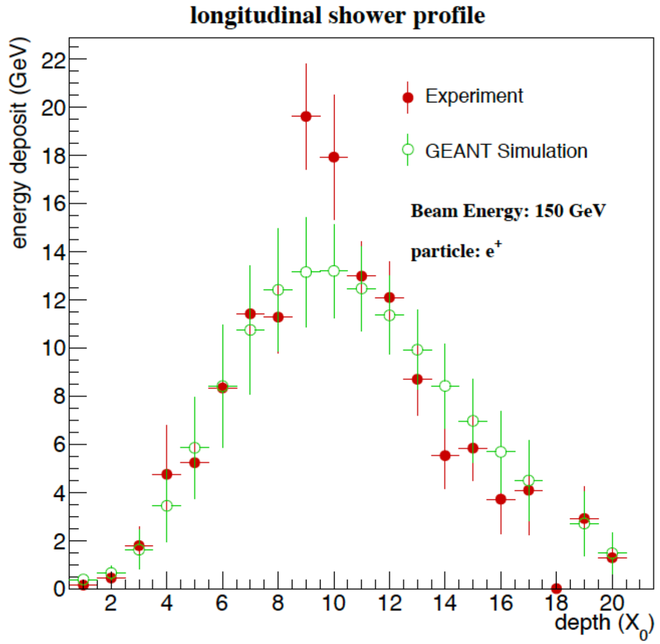




(b) Hit selection and clustering



(c) Longitudinal summing and E, hit position determinations

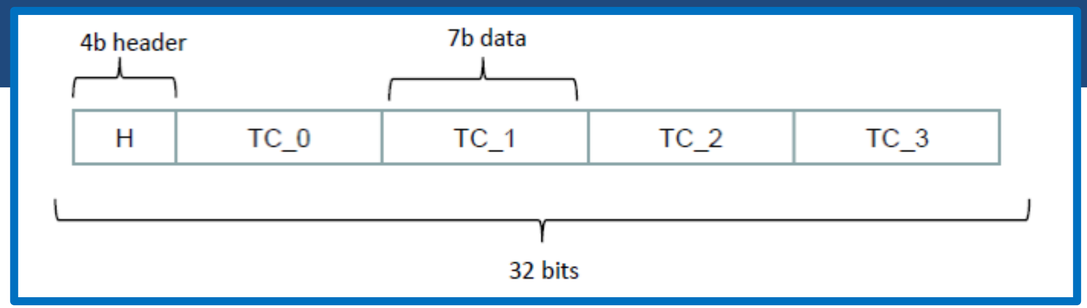


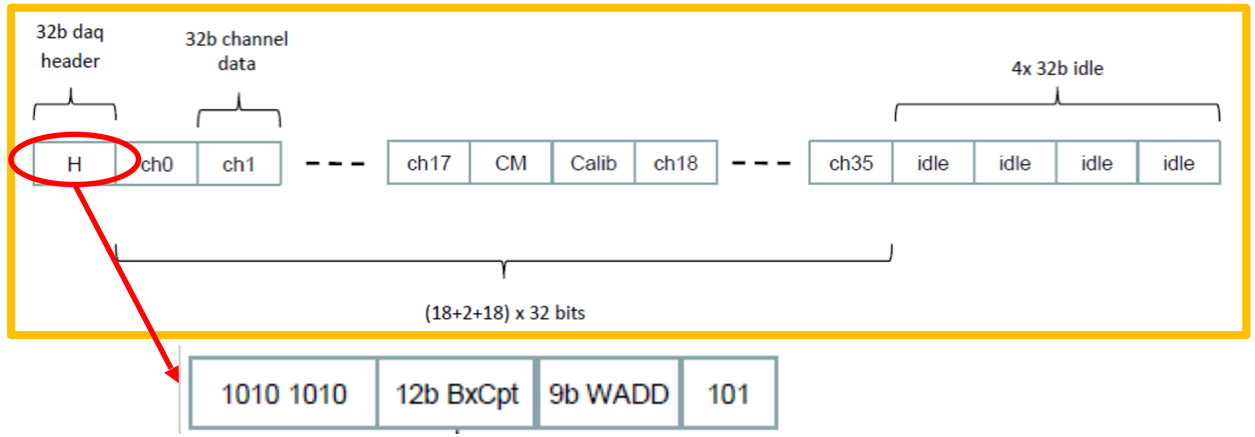
Figures from Y. Minato
(Nara Women's Univ.),Master thesis (2020)

BACK UP

HGCROC: DATA FORMAT

- Trigger charge sum (TC_X) produced @40MHz and transferred @1.28Gb/s
- Data @1.28Gb/s
  - Local trigger information used to request data transfer (L1 message)
  - The full frame is transferred for each L1 message
  - No individual channel selection is possible





Total of 32b + (18+2+18)x32b + 4x32b = 1376b

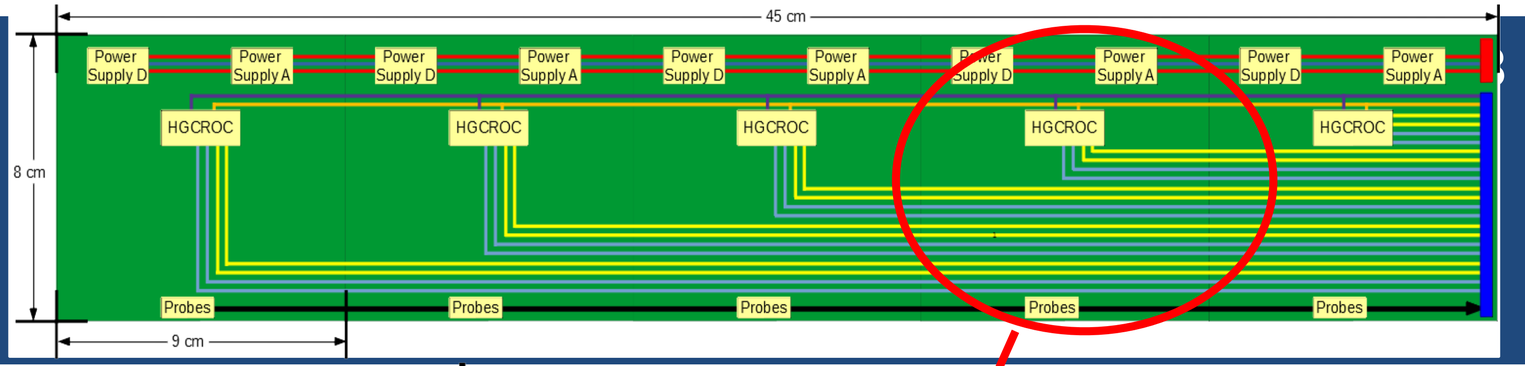
→ to be readout at 1.28Gb/s → 1.075 µs (≈930kHz)

Time between 2 successive local-L1-Trigger

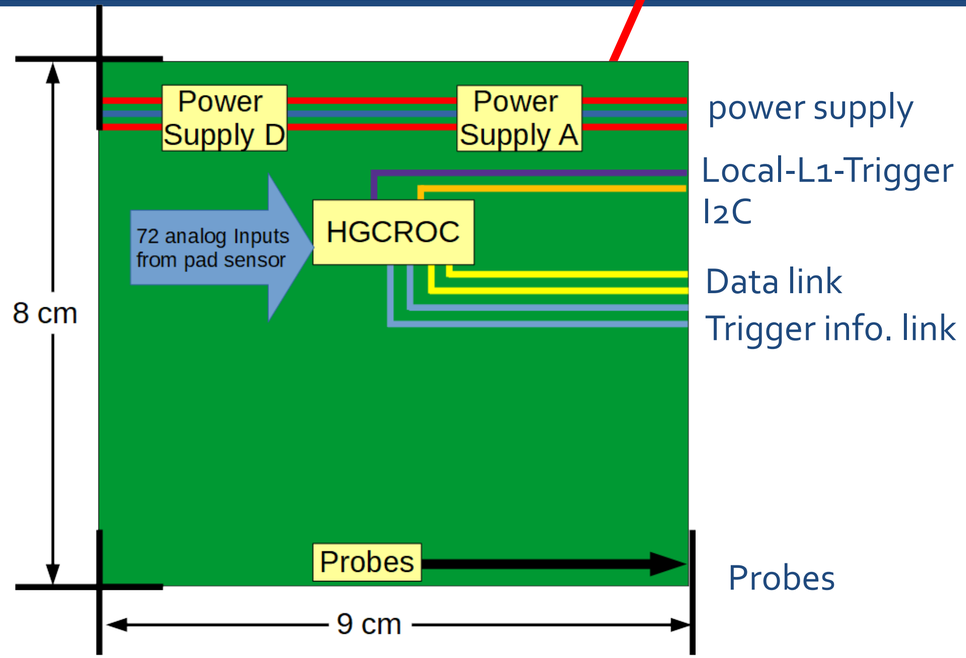
Close to 1MHz for read out detector

Slides by F. Rarbi at FoCal review (2020)

PAD-LAYER: PROPOSED FEE ARCHITECTURE

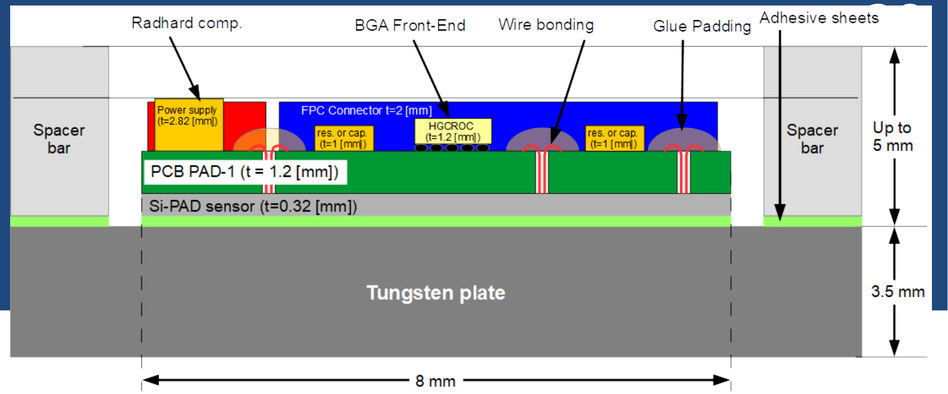


- FEE architecture :
  - PCB of 8 x 45 cm² with 5 embedded "HGCROC"
  - Analog signals from each pad sensors (72 pixels) will be read out by the HGCROC front-end chip which includes a charge sensitive amplifier-shaper and digitized to ship the data on a standard digital connection
  - Probes:
    - Temperature
    - Analog Power consumption
    - Digital Power consumption
  - Local power converter for cleaning power supplies



- **ASIC HGCROC**
  - BGA packaging
  - 78 channels,
    - 2 serial data link @1.28Gb/s
    - 2 serial Trigger link @1.28Gb/s ➔ Generated by HGCROC
  - Analog power supply (1.2V) (10mW/ch.)
  - Digital power supply (1.2V) (5mW/ch.)

PAD-LAYER DESIGN: TEMPERATURE SIMULATION



- Heat dissipation through ANSYS simulation, RT=20°C:
  - ONE full pad-layer including W plate, Si-pad and PCB FEE board with embedded HGCROC chips
  - PCB enclosed between 2 successive W plates
  - 1mm thickness sheet of copper used for passive cooling
  - Temperature variation for cooling from 0 °C up to 30°C
  - Hot spot @ center of HGCROC