

# LLVM + MLIR + CIRCT: A golden age of HLS?

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Masanori Ogino

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Hiroshima University, Experimental Quark Physics Laboratory, Computing Team

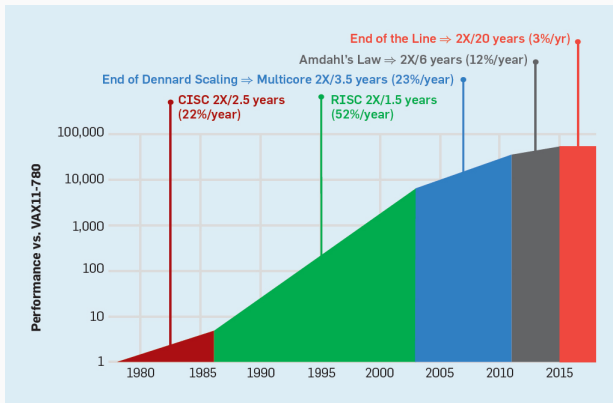
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# Heterogeneous Computing

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# Is Free Lunch Finally Over?



**Figure 1:** Growth of computer performance using integer programs (SPECintCPU), cited from J. L. Hennessy and D. A. Patterson, “A New Golden Age for Computer Architecture”, CACM Feb. 2019.

# The Age of Heterogeneous Computing

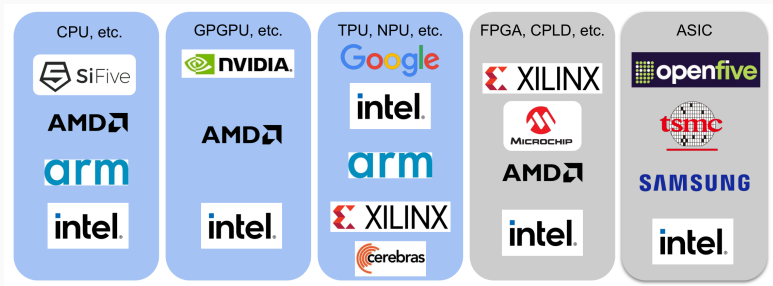


Figure 2: Major players on heterogeneous computing market, cited from C. Lattner, “The Golden Age of Compilers in an era of Hardware/Software co-design”, ASPLOS 2021.

# A Big Problem: Fragmentation of Tools, Languages, ...



Figure 3: Tools around heterogeneous computing, cited from C. Lattner, “The Golden Age of Compilers in an era of Hardware/Software co-design”, ASPLOS 2021.

LLVM

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# What Is LLVM?





## What Is LLVM?

- A **modular** compiler toolkit
- **Intermediate representation (IR)** for abstract CPU
- Can use for **SIMT GPGPU**
- Not good for **massively parallel accelerators** (TPU, NPU, ...)

MLIR

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# What is MLIR?



# What Is MLIR?

- A toolkit for **designing IRs**
- **Conversion** between different **abstraction levels**
- Define IRs for GPU, TPU, NPU, ... by **ourselves**
- Even LLVM IR could be defined on top of MLIR

CIRCT

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# What Is CIRCT?

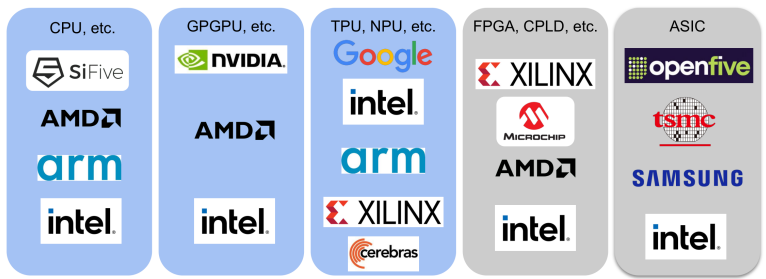
The logo for CIRCT is displayed in a dark gray, bold, sans-serif font on a white background. The letters 'C', 'I', and 'R' are arranged in a top row, while 'C', 'T', and 'R' are arranged in a bottom row. The 'C' in the bottom row is significantly larger than the other letters, extending to the left and partially overlapping the 'I' and 'R' of the top row. The 'I' and 'R' in the top row are positioned above the 'T' and 'R' in the bottom row, respectively. The overall layout is a stylized representation of the acronym CIRCT.

CIRCT

# What Is MLIR?

- IRs for **describing digital circuits** on top of MLIR
- Affine, sequential, combinational, ...

# A Foundation of Heterogeneous Computing



LLVM + MLIR + CIRCT

A foundation of next-generation programming environment?



HLS

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# HLS: A Territory of C

**Table 1:** Overview of high-level synthesis tools, cited from R. Nane et al., “A Survey and Evaluation of FPGA High-Level Synthesis Tools”, TCAD 2015.

Status	Compiler	Owner	License	Input	Output	Year	Domain	TestBench	FP	FixP	
In Use	eXcite	Y Explorations	Commercial	C	VHDL/Verilog	2001	All	Yes	No	Yes	
	CoDeveloper	Impulse Accelerated	Commercial	Impulse-C	VHDL/Verilog	2003	Image Streaming	Yes	Yes	No	
	Catapult-C	Calypto Design Systems	Commercial	C/C++ SystemC	VHDL/Verilog SystemC	2004	All	Yes	No	Yes	
	Cynthiesizer	FORTE	Commercial	SystemC	Verilog	2004	All	Yes	Yes	Yes	
	Bluespec	Bluespec Inc.	Commercial	BSV	System Verilog	2007	All	No	No	No	
	CHC	Allium	Commercial	C subset	VHDL/Verilog	2008	All	No	Yes	Yes	
	CtoS	Cadence	Commercial	SystemC TLM/C++	Verilog SystemC	2008	All	Only cycle accurate	No	Yes	
	DK Design Suite	Mentor Graphics	Commercial	Handel-C	VHDL/Verilog	2009	Streaming	No	No	Yes	
	GAUT	U. Bretagne	Academic	C/C++	VHDL	2010	DSP	Yes	No	Yes	
	MaxCompiler	Maxeler	Commercial	MaxJ	RTL	2010	DataFlow	No	Yes	No	
	ROCC	Jacquard Comp.	Commercial	C subset	VHDL	2010	Streaming	No	Yes	No	
	Symphony C	Synopsys	Commercial	C/C++	VHDL/Verilog SystemC	2010	All	Yes	No	Yes	
	Cyber-WorkBench	NEC	Commercial	BDL	VHDL/Verilog	2011	All	Cycle/Formal	Yes	Yes	
	LegUp	U. Toronto	Academic	C	Verilog	2011	All	Yes	No	No	
	Bambu	Polimi	Academic	C	Verilog	2012	All	Yes	Yes	No	
	DWARV	TU. Delft	Academic	C subset	VHDL	2012	All	Yes	Yes	Yes	
	VivadoHLS	Xilinx	Commercial	C/C++ SystemC	VHDL/Verilog SystemC	2013	All	Yes	Yes	Yes	
	N/A	Trident	Los Alamos NL	Academic	C subset	VHDL	2007	Scientific	No	Yes	No
		CHIMPS	U. Washington	Academic	C	VHDL	2008	All	No	No	No
Krwi		U. Cambridge	Academic	C#	Verilog	2008	.NET	No	No	No	
gcc2verilog [45]		U. Korea	Academic	C	Verilog	2011	All	No	No	No	
HercuLeS		Ajax Compiler	Commercial	C/NAC	VHDL	2012	All	Yes	Yes	Yes	
Napa-C		Sarnoff Corp.	Academic	C subset	VHDL/Verilog	1998	Loop	No	No	No	
Abandoned	DEFACITO	U. South Calif.	Academic	C	RTL	1999	DSE	No	No	No	
	Garp	U. Berkeley	Academic	C subset	bitstream	2000	Loop	No	No	No	
	MATCH	U. Northwest	Academic	MATLAB	VHDL	2000	Image	No	No	No	
	PipeRench	U. Carnegie M.	Academic	DIL	bitstream	2000	Stream	No	No	No	
	SeaCucumber	U. Brigham Y.	Academic	Java	EDIP	2002	All	No	Yes	Yes	
	SA-C	U. Colorado	Academic	SA-C	VHDL	2003	Image	No	No	No	
	SPARK	U. Cal. Irvine	Academic	C	VHDL	2003	Control	No	No	No	
	AccelDSP	Xilinx	Commercial	MATLAB	VHDL/Verilog	2006	DSP	Yes	Yes	Yes	
	C2H	Altera	Commercial	C	VHDL/Verilog	2006	All	No	No	No	
	CtoVerilog	U. Haifa	Academic	C	Verilog	2008	All	No	No	No	

# Idea: Turning LLVM-based programming language(s) into HLS language(s)?

- LLVM-based compiler is everywhere
- C, C++, Fortran, Rust, Swift, Julia, Common Lisp, Haskell, TensorFlow, ...
- Use those powerful languages into HLS with MLIR and CIRCT?

# Conclusion

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# Conclusion

- Fragmentation of tools and languages
- Re-implementation and reinvent again and again
- LLVM + MLIR + CIRCT: a breakthrough?
- HLS with something better than C?

QUESTIONS, SUGGESTIONS, CORRECTIONS, WHATEVER?

THANK YOU FOR ATTENDING!